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**UTILITY
PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. MI22-1035 Total Pages 77

First Named Inventor or Application Identifier

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

1. <input checked="" type="checkbox"/> Fee Transmittal Form (Submit an original, and a duplicate for fee processing)	6. <input type="checkbox"/> Microfiche Computer Program (Appendix)
2. <input checked="" type="checkbox"/> Specification [Total Pages 23] (preferred arrangement set forth below)	7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
- Descriptive title of the Invention <u>PLUS TITLE PAGE</u>	
- Cross References to Related Applications	
- Statement Regarding Fed sponsored R & D	
- Reference to Microfiche Appendix	
- Background of the Invention	
- Brief Summary of the Invention	
- Brief Description of the Drawings (if filed)	
- Detailed Description	
- Claim(s)	
- Abstract of the Disclosure	
3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) [Total Sheets 4] (Figs. 1-8)	8. <input checked="" type="checkbox"/> Assignment Papers (cover sheet & document(s))
4. Oath or Declaration [Total Pages 2]	9. <input type="checkbox"/> 37 CFR 3.73(b) Statement <input type="checkbox"/> Power of Attorney (when there is an assignee)
a. <input checked="" type="checkbox"/> Newly executed (original or copy)	10. <input type="checkbox"/> English Translation Document (if applicable)
b. <input type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 17 completed) <i>[Note Box 5 below]</i>	11. <input checked="" type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input checked="" type="checkbox"/> Copies of IDS Citations
i. <input type="checkbox"/> <u>DELETION OF INVENTOR(S)</u> Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).	
5. <input type="checkbox"/> Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.	12. <input type="checkbox"/> Preliminary Amendment
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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SEMICONDUCTOR PROCESSING METHODS

* * * * *

INVENTORS

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ATTORNEY'S DOCKET NO. MI22-1035

SEMICONDUCTOR PROCESSING METHODS

TECHNICAL FIELD

The invention pertains to semiconductor processing methods, and particularly pertains to methods of removing some portions of a layer from over a semiconductive substrate, while leaving other portions of the layer remaining over the substrate.

BACKGROUND OF THE INVENTION

Modern semiconductor processing frequently involves photolithographic methods to pattern materials into very small structures, which are ultimately incorporated into a semiconductor circuit. An exemplary prior art method for forming small structures from a layer of material is as follows. First, the layer of material is provided over a semiconductive substrate. Subsequently, a layer of photoresist is provided over the layer of material. A photolithographic mask is then provided over the layer of photoresist and light is shined through the mask to expose portions of the layer of photoresist while leaving other portions unexposed. The photoresist typically comprises an unsaturated organic material, such as, for example, a material comprising one or more unsaturated carbon-containing rings. The exposed portions are rendered either more or less soluble in a solvent relative to the unexposed portions. If the exposed portions are rendered more soluble,

1 the resist is referred to as a positive photoresist (as a positive image
2 of a pattern from the photolithographic mask is transferred to the
3 photoresist), and if the exposed portions are rendered less soluble, the
4 photoresist is referred to as a negative photoresist (as a negative image
5 of the pattern from the photolithographic mask is transferred to the
6 photoresist). In any event, the photoresist is exposed to a solvent and
7 either the exposed or unexposed portions are removed while leaving the
8 other of the exposed or unexposed portions remaining over the layer of
9 material. Such patterns the photoresist into a patterned mask overlaying
10 the layer of material. The layer of material is then exposed to
11 conditions which transfer a pattern from the patterned mask to the
12 layer of material (i.e., which removes portions of the layer of material
13 not covered by photoresist, while leaving the portions of the layer
14 material that are covered by photoresist). Subsequently, the photoresist
15 is removed and the substrate having the patterned layer of material
16 thereon is subjected to subsequent processing steps to form an
17 integrated circuit over the substrate.

18 Typically, the semiconductive substrate referred to above is in the
19 form of a wafer and a plurality of semiconductor packages (i.e.,
20 individual integrated circuits) are simultaneously formed over the wafer.
21 After the formation of the plurality of semiconductor packages is
22 complete, the wafer is subjected to a die-cutting process to separate the
23 individual integrated circuits from one another. In wafer fabrication

1 processes employed to date, photoresist is entirely removed from a wafer
2 prior to subjecting the wafer to a die-cutting process. Among the
3 reasons for removal of the photoresist is that the photoresist is not a
4 material suitable for incorporation into semiconductor circuits. It would
5 be desirable to develop alternative methods for patterning structures
6 during semiconductor circuit fabrication processes.

7 In an area of semiconductor processing considered to be unrelated
8 to the above-described photolithographic processing methods, a recently
9 developed technique for forming insulative materials is Flowfill™
10 Technology, which has been developed by Trikon Technology of Bristol,
11 U.K. The process can be utilized for forming either silicon dioxide or
12 methylsilicon oxide ($(CH_3)_xSiO_{2-x}$), for example. The process for forming
13 silicon dioxide is as follows. First, SiH_4 and H_2O_2 are separately
14 introduced into a chemical vapor deposition (CVD) chamber, such as a
15 parallel plate reaction chamber. The reaction rate between SiH_4 and
16 H_2O_2 can be moderated by the introduction of nitrogen into the reaction
17 chamber. A semiconductive wafer is provided within the chamber, and
18 ideally maintained at a suitably low temperature, such as 0°C, at an
19 exemplary pressure of 1 Torr to achieve formation of a silanol-type
20 structure of the formula $Si(OH)_x$, which is predominantly $Si(OH)_4$. The
21 $Si(OH)_4$ condenses onto the wafer surface. Although the reaction occurs
22 in the gas phase, the deposited $Si(OH)_4$ is in the form of a viscous
23 liquid which flows to fill small gaps on the wafer surface. In

1 applications where deposition thickness increases, surface tension drives
2 the deposited layer flat, thus forming a planarized layer over the
3 substrate.

4 The liquid $\text{Si}(\text{OH})_4$ is typically converted to a silicon dioxide
5 structure by a two-step process. First, planarization of the liquid film
6 is promoted by increasing the temperature to above 100°C, while
7 maintaining the pressure of about 1 Torr, to result in solidification and
8 formation of a polymer layer. Thereafter, the temperature is raised to
9 above 400°C, while maintaining the pressure of greater than 1 Torr, to
10 form SiO_2 . The processing above 400°C also provides the advantage of
11 driving undesired water from the resultant SiO_2 layer.

12 The formation of methylsilicon oxide is accomplished similarly to
13 that described above for forming silicon dioxide, with the exception that
14 methylsilane $((\text{CH}_3)_z\text{SiH}_{4-z})$, wherein z is at least 1 and no greater
15 than 4) is combined with the hydrogen peroxide to produce a
16 methylsilanol, instead of combining the silane (SiH_4) with the hydrogen
17 peroxide to form silanol.

18

19 **SUMMARY OF THE INVENTION**

20 In one aspect, the invention encompasses a semiconductor
21 processing method wherein a layer of material is formed over a
22 semiconductive wafer substrate. Some portions of the layer are exposed
23 to energy while other portions are not exposed. The exposure to

1 energy alters physical properties of the exposed portions relative to the
2 unexposed portions. After the portions are exposed, the exposed and
3 unexposed portions of the layer are subjected to common conditions.
4 The common conditions are effective to remove the material and
5 comprise a rate of removal that is influenced by the altered physical
6 properties of the layer. The common conditions remove either the
7 exposed or unexposed portions faster than the other of the exposed and
8 unexposed portions. After the selective removal of the exposed or
9 unexposed portions, and while the other of the exposed and unexposed
10 portions remains over the substrate, the wafer is cut into separated die.

11 In another aspect, the invention encompasses another
12 semiconductor processing method. A layer of $(CH_3)_ySi(OH)_{4-y}$ is formed
13 over a substrate, wherein y is greater than 0 and less than 4. Some
14 portions of the layer are exposed to ultraviolet light while other
15 portions are not exposed. The exposure to ultraviolet light converts the
16 exposed portions to $(CH_3)_xSiO_{2-x}$, wherein x is greater than 0 and less
17 than 2. After the exposure to ultraviolet light, the exposed and
18 unexposed portions of the layer are subjected to hydrofluoric acid to
19 selectively remove the $(CH_3)_ySi(OH)_{4-y}$ of the unexposed portions relative
20 to the $(CH_3)_xSiO_{2-x}$ of the exposed portions.

21

22

23

1 BRIEF DESCRIPTION OF THE DRAWINGS

2 Preferred embodiments of the invention are described below with
3 reference to the following accompanying drawings.

4 Fig. 1 is a fragmentary, diagrammatic, cross-sectional view of a
5 semiconductive wafer fragment at a first step of a processing method in
6 accordance with the present invention.

7 Fig. 2 is a view of the Fig. 1 wafer fragment at a step subsequent
8 to that of Fig. 1.

9 Fig. 3 is a view of the Fig. 1 wafer fragment at a step subsequent
10 to that of Fig. 2 in accordance with a first embodiment processing
11 method of the present invention.

12 Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step
13 subsequent to that of Fig. 3.

14 Fig. 5 is a view of the Fig. 1 wafer fragment shown at a step
15 subsequent to that of Fig. 2, and in accordance with a second
16 embodiment processing sequence of the present invention.

17 Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step
18 subsequent to that of Fig. 5.

19 Fig. 7 is a top view of a semiconductive wafer, such as the wafer
20 incorporating the fragment of Fig. 1, shown prior to subjecting the
21 wafer to a die-cutting process.

22 Fig. 8 is a top view of portions of the Fig. 7 semiconductive
23 wafer shown after the wafer is subjected to a die-cutting process.

1 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

2 This disclosure of the invention is submitted in furtherance of the
3 constitutional purposes of the U.S. Patent Laws "to promote the
4 progress of science and useful arts" (Article 1, Section 8).

5 The invention encompasses methods for utilizing energy to form
6 patterned masking materials on a wafer. In particular aspects of the
7 invention, the patterned masking materials are retained on a wafer after
8 a die-cutting process. In other particular aspects of the invention, the
9 patterned masking materials comprise silicon. The invention is described
10 with reference to a preferred embodiment in Figs. 1-8.

11 Referring to Fig. 1, a semiconductive wafer fragment 10 is
12 illustrated at a preliminary step of a processing sequence encompassed
13 by the present invention. Wafer fragment 10 comprises a
14 semiconductive substrate 12. Substrate 12 can comprise, for example,
15 monocrystalline silicon lightly doped with a p-type conductivity enhancing
16 dopant. To aid in interpretation of the claims that follow, the term
17 "semiconductive substrate" is defined to mean any construction
18 comprising semiconductive material, including, but not limited to, bulk
19 semiconductive materials such as a semiconductive wafer (either alone
20 or in assemblies comprising other materials thereon), and semiconductive
21 material layers (either alone or in assemblies comprising other
22 materials). The term "substrate" refers to any supporting structure,
23

1 including, but not limited to, the semiconductive substrates described
2 above.

3 A first layer of material 14 is formed over substrate 12, and a
4 second layer of material 16 is formed over first layer 14. The material
5 of first layer 14 can be either a conductive material or an insulative
6 material, and is not particularly germane to the present invention. The
7 material of second layer 16 has physical properties which can be altered
8 by exposure to energy. The material of second layer 16 can comprise,
9 for example, methylsilanol $((CH_3)_ySi(OH)_{4-y})$ or silanol $(Si(OH)_4)$, either
10 of which can be formed by methods described above in the
11 "Background" section of this disclosure. Both methylsilanol and silanol
12 have physical properties which can be altered by exposure to, for
13 example, electron beam energy, ultraviolet light or plasma. For
14 instance, if portions of either silanol or methylsilanol are exposed to
15 ultraviolet light, such portions will have a higher etch rate in
16 hydrofluoric acid than will portions not exposed to the ultraviolet light.
17 The exposure of methylsilanol to ultraviolet light converts it to the
18 insulative material $(CH_3)_xSiO_{2-x}$, and exposure of silanol to ultraviolet
19 light converts it silicon dioxide.

20 Referring to Fig. 2, an energy source 18 is provided over wafer
21 fragment 10, and a patterned photolithographic mask 20 is provided
22 between source 18 and second layer 16. Mask 20 comprises orifices 22
23 extending therethrough. In operation, energy 24 is emitted from

1 source 18 and toward mask 20. In the illustrated embodiment, the
2 energy is shown as light waves which can comprise, for example,
3 wavelengths corresponding to ultraviolet light. Mask 20 blocks some of
4 the light waves, while other light waves penetrate through orifices 22 to
5 reach layer 16. Layer 16 is thus divided into portions 30 which are
6 exposed to the radiation from source 18 and portions 32 which are
7 shielded by mask 20 and not exposed to radiation 24. The exposure of
8 layer 16 to radiation 24 alters physical properties of the material of
9 layer 16 within exposed regions 30 relative to physical properties of the
10 material in unexposed portions 32.

11 After the exposure to radiation 24, the exposed portions 30 and
12 unexposed portions 32 of layer 16 are exposed to common conditions
13 which are effective to remove the material of layer 16. Further, the
14 common conditions comprise a rate of removal of the material of
15 layer 16 that is influenced by physical properties altered by exposure to
16 radiation 24. Accordingly, exposed portions 30 are removed at a
17 different rate than unexposed portions 32. Figs. 3 and 4 illustrate an
18 embodiment wherein exposed portions 30 are removed at a slower rate
19 than unexposed portions 32, and Figs. 5 and 6 illustrate an embodiment
20 wherein the exposed portions are removed at a faster rate than the
21 unexposed portions.

22 Referring first to the embodiment of Figs. 3 and 4, and
23 specifically referring to Fig. 3, substrate 10 is illustrated after exposure

1 to conditions which remove exposed portions 32 (Fig. 2) more rapidly
2 than unexposed portions 30, to leave only unexposed portions 30
3 remaining over first material 14. In an exemplary embodiment, the
4 material of layer 16 can comprise either methylsilanol or silanol, the
5 radiation 24 (Fig. 2) can comprise ultraviolet light, and the common
6 conditions can comprise exposure to hydrofluoric acid. The ultraviolet
7 light converts exposed material of layer 16 to either methylsilicon
8 dioxide or silicon dioxide, and thus renders such exposed portions more
9 resistant to hydrofluoric acid removal than unexposed portions
10 comprising either methylsilanol or silanol. In the exemplary
11 embodiment, it is found that the portions of a methylsilanol or silanol
12 layer 16 exposed to ultraviolet light are removed by hydrofluoric acid
13 at a rate that is at least about 5 times slower than portions of layer 16
14 not exposed to ultraviolet light. The portions not exposed to ultraviolet
15 light can thus be selectively removed relative to the portions that have
16 been exposed to ultraviolet light. For purposes of interpreting this
17 disclosure and the claims that follow, a first material is "selectively
18 removed" relative to another material if the first material is removed
19 at a rate that is at least 3 times faster than a rate at which the other
20 material is removed.

21 Referring to Fig. 4, a pattern is transferred from exposed
22 portions 30 to underlying layer 14. Specifically, portions of layer 14 are
23 removed by an etch. The conditions of the etch will vary depending

1 on the material of layer 14, and can comprise conventional methods
2 which will be recognized by persons of ordinary skill in the art for
3 utilization with various materials of layer 14.

4 Referring to 5 and 6, processing similar to that of Figs. 3 and 4
5 is illustrated with the exception that it is exposed portions 30 (Fig. 2)
6 that have a faster rate of removal than unexposed portions 32 when
7 layer 16 is subjected to conditions for removing the material of
8 layer 16.

9 An advantage of the present invention relative to prior art
10 methods described above in the "Background" section of this disclosure
11 is that the photolithographically patterned layer 16 does not comprise
12 photoresist. Accordingly, layer 16 can have attributes desired in
13 structures formed over substrate 12. For instance, in the above-
14 described exemplary embodiment of Figs. 3 and 4, the remaining
15 portions 30 of layer 16 comprise an insulative material (either silicon
16 dioxide or methylsilicon oxide). Such insulative material can be utilized
17 for separating conductive components of a semiconductor circuit from
18 one another. In some applications, the methylsilicon oxide can be more
19 preferred than the silicon dioxide, as methylsilicon oxide has a lower
20 dielectric constant than silicon oxide. Accordingly, methylsilicon oxide
21 can reduce parasitic capacitance between adjacent conductive components
22 relative to silicon dioxide. The advantages of utilizing methylsilicon
23 oxide can be generally realized from silicon oxides having the generic

1 formula R-Si-O, wherein R is an organic group. R can comprise, for
2 example, a hydrocarbon group.

3 Figs. 7 and 8 illustrate subsequent processing which can occur
4 after the processing of either Figs. 3 and 4, or the processing of Figs. 5
5 and 6. Specifically, Fig. 7 is a view of an entirety of a semiconductive
6 wafer 50 which has been processed. The semiconductive wafer has a
7 plurality of semiconductor structures (e.g., circuitry) formed thereover
8 (not shown) and is subdivided into circuit packages 52 (only some of
9 which are labeled). Imaginary dashed lines 53 are provided to show
10 boundaries between adjacent semiconductor circuit packages 52. For
11 reasons discussed above, structures comprised by packages 52 can
12 comprise portions of photolithographically patterned layer 16
13 incorporated therein.

14 Referring to Fig. 8, wafer fragment 50 (Fig. 7) is illustrated after
15 being subjected to a die-cutting process, wherein the wafer has been cut
16 into separated die corresponding to packages 52.

17 In compliance with the statute, the invention has been described
18 in language more or less specific as to structural and methodical
19 features. It is to be understood, however, that the invention is not
20 limited to the specific features shown and described, since the means
21 herein disclosed comprise preferred forms of putting the invention into
22 effect. The invention is, therefore, claimed in any of its forms or
23

modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

1 **CLAIMS:**

2 1. A semiconductor processing method, comprising:
3 forming a layer of material over a semiconductive wafer substrate;
4 exposing some portions of the layer to energy while leaving other
5 portions unexposed, the exposing altering physical properties of the
6 exposed portions of material relative to the unexposed portions of
7 material;

8 after the exposing, subjecting the exposed and unexposed portions
9 of the layer to common conditions, the common conditions being
10 effective to remove the material and comprising a rate of removal that
11 is influenced by the altered physical properties of the layer, the common
12 conditions removing either the exposed or unexposed portions faster
13 than the other of the exposed and unexposed portions; and

14 after the selective removal of the exposed or unexposed portions,
15 and while the other of the exposed and unexposed portions remains
16 over the substrate, cutting the wafer into separated die.

17
18 2. The method of claim 1 wherein material comprises silicon.

19
20 3. The method of claim 1 wherein the material comprises
21 carbon, silicon and oxygen.

1 4. The method of claim 1 wherein the material comprises
2 silicon bound to a hydrocarbon group and bound to oxygen.

3
4 5. The method of claim 1 wherein the material comprises
5 $(CH_3)_ySi(OH)_{4-y}$, with y being greater than 0 and less than 4.

6
7 6. The method of claim 1 wherein the material comprises
8 $Si(OH)_4$.

9
10 7. The method of claim 1 wherein the energy is in the form
11 of ultraviolet light.

12
13 8. The method of claim 1 wherein the energy is in the form
14 of an electron beam.

15
16 9. The method of claim 1 wherein the energy is in the form
17 of a plasma.

1 10. A semiconductor processing method, comprising:
2 forming a layer of a silicon-comprising material over a substrate;
3 exposing some portions of the layer to energy while leaving other
4 portions unexposed, the exposing altering physical properties of the
5 exposed portions relative to the unexposed portions; and
6 after the exposing, subjecting the exposed and unexposed portions
7 of the layer to common conditions, the common conditions being
8 effective to remove the silicon-comprising material and comprising a rate
9 of removal that is influenced by the altered physical properties of the
10 layer, the common conditions removing either the exposed or unexposed
11 portions faster than the other of the exposed and unexposed portions.

12
13 11. The method of claim 10 wherein the silicon-comprising
14 material comprises carbon, silicon and oxygen.

15
16 12. The method of claim 10 wherein the silicon-comprising
17 material comprises silicon bound to a hydrocarbon group and bound to
18 oxygen.

1 13. The method of claim 10 wherein the silicon-comprising
2 material comprises silicon bound to a hydrocarbon group and bound to
3 oxygen, and wherein the hydrocarbon group does not comprise a carbon-
4 containing ring.

5
6 14. The method of claim 10 wherein the silicon-comprising
7 material comprises $(CH_3)_ySi(OH)_{4-y}$, with y being greater than 0 and less
8 than 4.

9
10 15. The method of claim 10 wherein the silicon-comprising
11 material comprises $Si(OH)_4$.

12
13 16. The method of claim 10 wherein the energy is in the form
14 of ultraviolet light.

15
16 17. The method of claim 10 wherein the energy is in the form
17 of an electron beam.

18
19 18. The method of claim 10 wherein the energy is in the form
20 of a plasma.

1 19. The method of claim 10 wherein the silicon-comprising
2 material comprises $(CH_3)_ySi(OH)_{4-y}$, with y being greater than 0 and less
3 than 4, and the energy is in the form of ultraviolet light; and wherein:

4 the exposing comprises passing the ultraviolet light through
5 openings in a patterned mask and onto the layer of material to expose
6 said some portions of the layer to the ultraviolet light while leaving said
7 other portions unexposed; and

8 the common conditions comprising subjecting the entire layer to
9 hydrofluoric acid, the hydrofluoric acid removing portions of the layer
10 that were not exposed to ultraviolet light at a faster rate than portions
11 of the layer that were exposed to ultraviolet light.

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1 20. The method of claim 10 wherein the silicon-comprising
2 material comprises Si(OH)_4 and the energy is in the form of ultraviolet
3 light; and wherein:

4 the exposing comprises passing the ultraviolet light through
5 openings in a patterned mask and onto the layer of material to expose
6 said some portions of the layer to the ultraviolet light while leaving said
7 other portions unexposed; and

8 the common conditions comprising subjecting the entire layer to
9 a solvent comprising hydrofluoric acid, the hydrofluoric acid removing
10 portions of the layer that were not exposed to ultraviolet light at a
11 faster rate than portions of the layer that were exposed to ultraviolet
12 light.

13

14 21. The method of claim 10 wherein the silicon-comprising
15 material comprises Si(OH)_4 and the energy is in the form of an electron
16 beam; and wherein:

17 the exposing comprises exposing said some portions of the layer
18 to the electron beam while leaving said other portions unexposed; and

19 the common conditions comprising subjecting the entire layer to
20 hydrofluoric acid, the hydrofluoric acid removing portions of the layer
21 that were not exposed to the electron beam at a faster rate than
22 portions of the layer that were exposed to the electron beam.

1 22. A semiconductor processing method, comprising:

2 forming a layer of $(CH_3)_ySi(OH)_{4-y}$, with y being greater than 0
3 and less than 4, over a substrate;

4 exposing some portions of the layer to ultraviolet light while
5 leaving other portions unexposed, the exposing converting the exposed
6 portions to $(CH_3)_xSiO_{2-x}$, with x being greater than 0 and less than 2;
7 and

8 after the exposing, subjecting the exposed and unexposed portions
9 of the layer to hydrofluoric acid to selectively remove the
10 $(CH_3)_ySi(OH)_{4-y}$ of the unexposed portions relative to the $(CH_3)_xSiO_{2-x}$ of
11 the exposed portions.

12
13 23. The method of claim 22 wherein the ultraviolet light is
14 passed onto the layer of $(CH_3)_ySi(OH)_{4-y}$ through openings in a
15 patterned mask.

16
17 24. The method of claim 22 wherein the substrate is a
18 semiconductive wafer, and further comprising:

19 after the selective removal of the $(CH_3)_ySi(OH)_{4-y}$ of the unexposed
20 portions, and while the $(CH_3)_xSiO_{2-x}$ of the exposed portions remains
21 over the substrate, cutting the wafer into separated die.

1 25. A semiconductor processing method, comprising:
2 forming a layer of $\text{Si}(\text{OH})_4$ over a substrate;
3 exposing some portions of the layer to energy while leaving other
4 portions unexposed, the exposing converting the exposed portions to
5 SiO_2 ; and

6 after the exposing, subjecting the exposed and unexposed portions
7 of the layer to hydrofluoric acid to selectively remove the $\text{Si}(\text{OH})_4$ of
8 the unexposed portions relative to the SiO_2 of the exposed portions.

9
10 26. The method of claim 25 wherein the energy is in the form
11 of ultraviolet light.

12
13 27. The method of claim 25 wherein the energy is in the form
14 of ultraviolet light and is passed onto the layer of $\text{Si}(\text{OH})_4$ through
15 openings in a patterned mask.

16
17 28. The method of claim 25 wherein the energy is in the form
18 of an electron beam.

1 29. The method of claim 25 wherein the substrate is a
2 semiconductive wafer, and further comprising:

3 after the selective removal of the $\text{Si}(\text{OH})_4$ of the unexposed
4 portions, and while the SiO_2 of the exposed portions remains over the
5 substrate, cutting the wafer into separated die.

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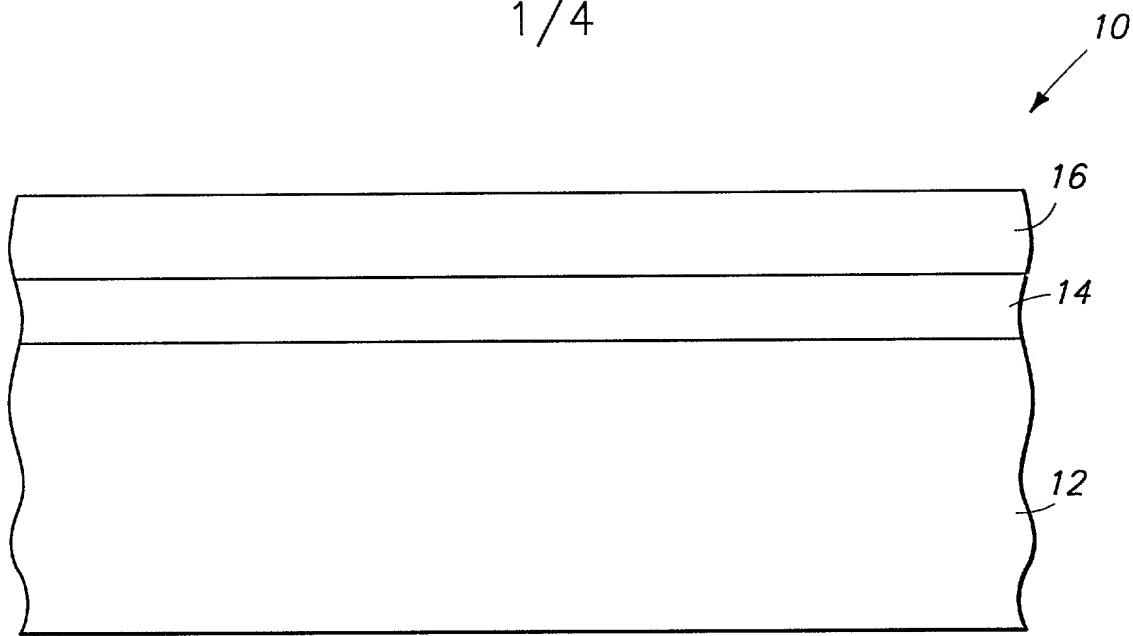
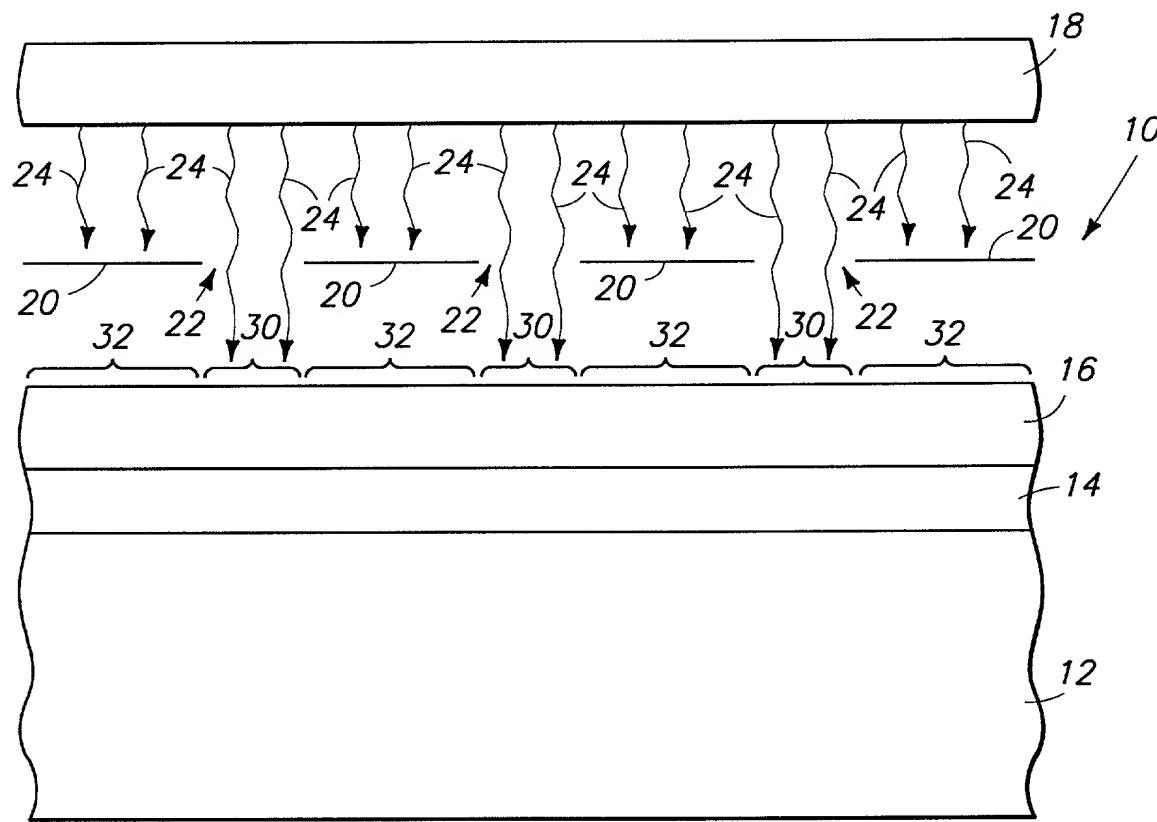
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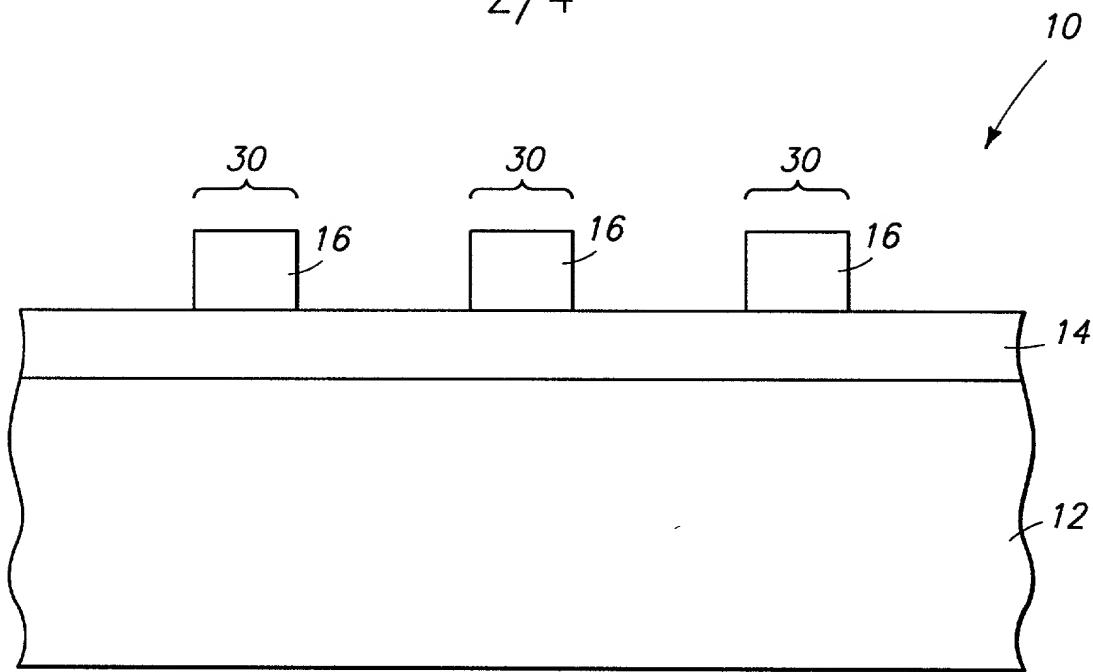
1 ABSTRACT OF THE DISCLOSURE

2 In one aspect, the invention encompasses a semiconductor
3 processing method. A layer of material is formed over a semiconductive
4 wafer substrate. Some portions of the layer are exposed to energy
5 while other portions are not exposed. The exposure to energy alters
6 physical properties of the exposed portions relative to the unexposed
7 portions. After the portions are exposed, the exposed and unexposed
8 portions of the layer are subjected to common conditions. The common
9 conditions are effective to remove the material and comprise a rate of
10 removal that is influenced by the altered physical properties of the
11 layer. The common conditions remove either the exposed or unexposed
12 portions faster than the other of the exposed and unexposed portions.
13 After the selective removal of the exposed or unexposed portions, and
14 while the other of the exposed and unexposed portions remains over the
15 substrate, the wafer is cut into separated die. In another aspect, the
16 invention encompasses another semiconductor processing method. A
17 layer of $(CH_3)_ySi(OH)_{4-y}$ is formed over a substrate. Some portions of
18 the layer are exposed to ultraviolet light while other portions are not
19 exposed. The exposure to ultraviolet light converts the exposed portions
20 to $(CH_3)_xSiO_{2-x}$. After the exposure to ultraviolet light, the exposed and
21 unexposed portions of the layer are subjected to hydrofluoric acid to
22 selectively remove the $(CH_3)_ySi(OH)_{4-y}$ of the unexposed portions relative
23 to the $(CH_3)_xSiO_{2-x}$ of the exposed portions.

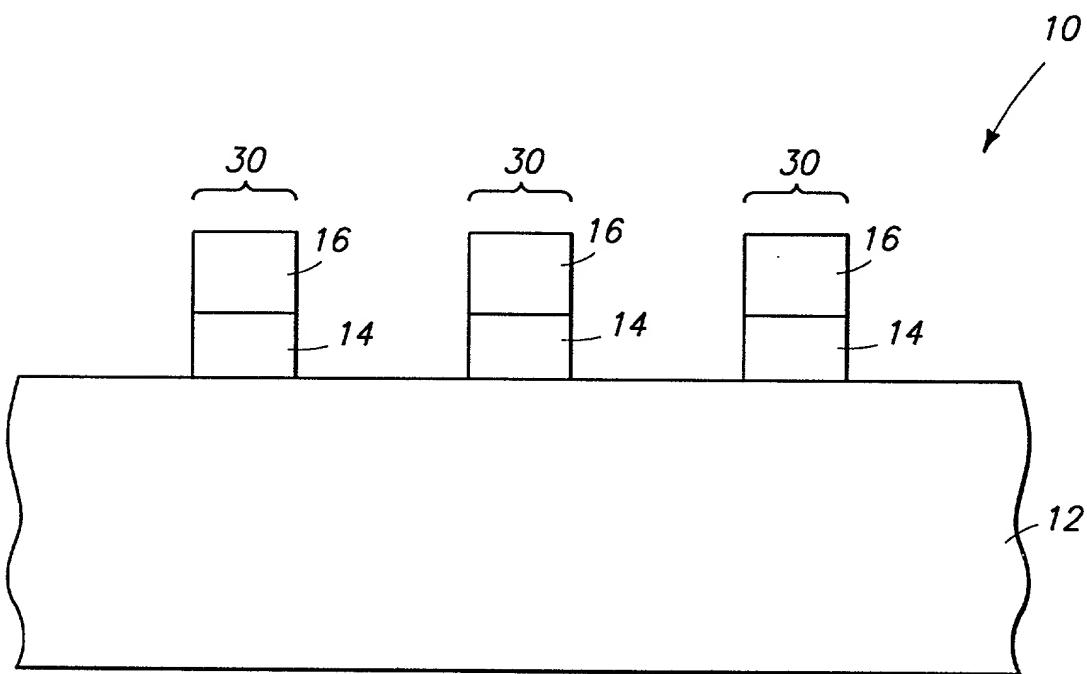
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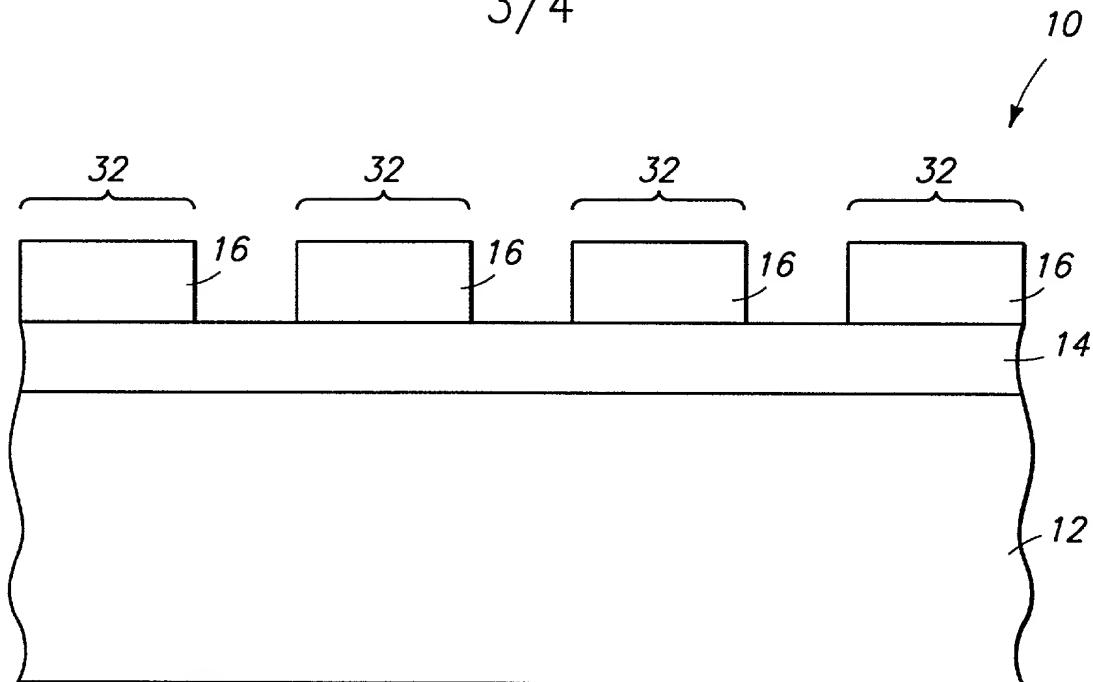
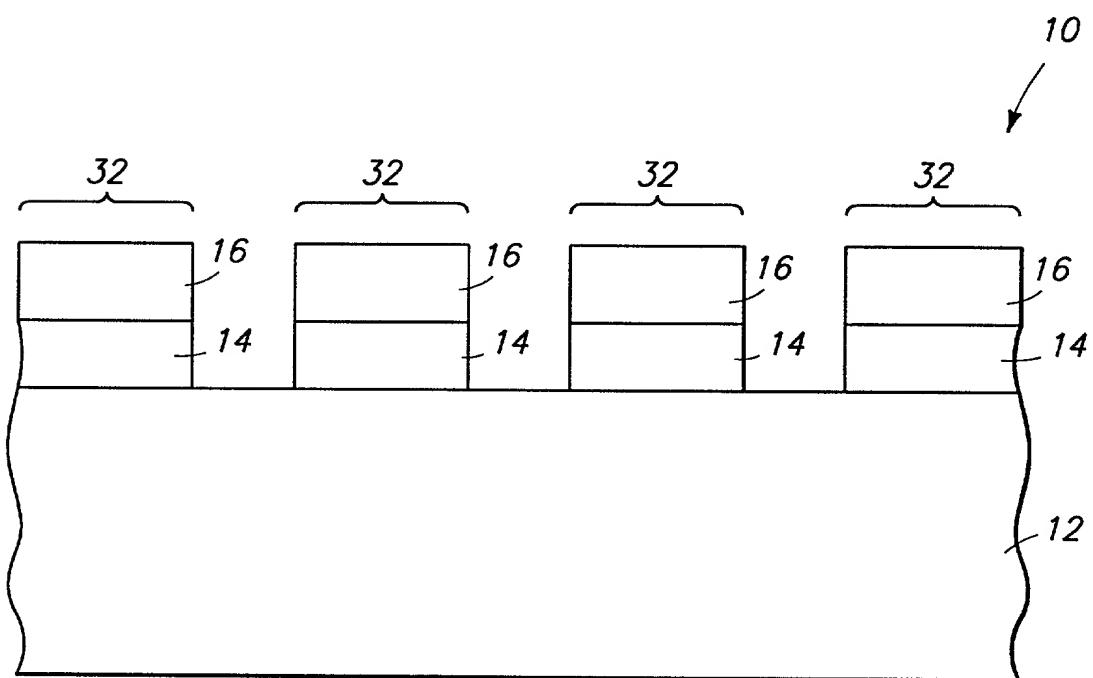


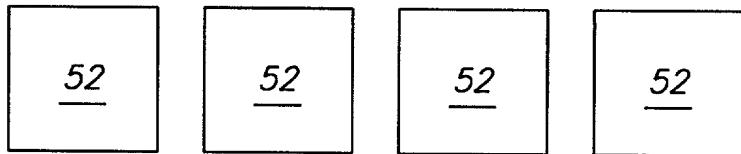
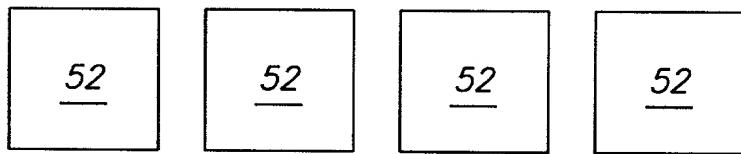
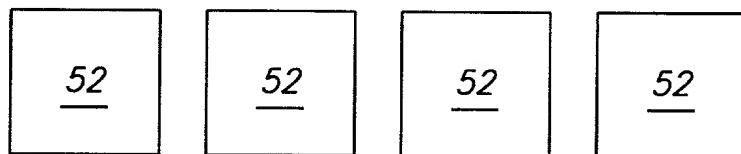
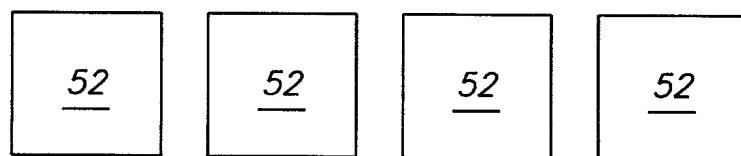
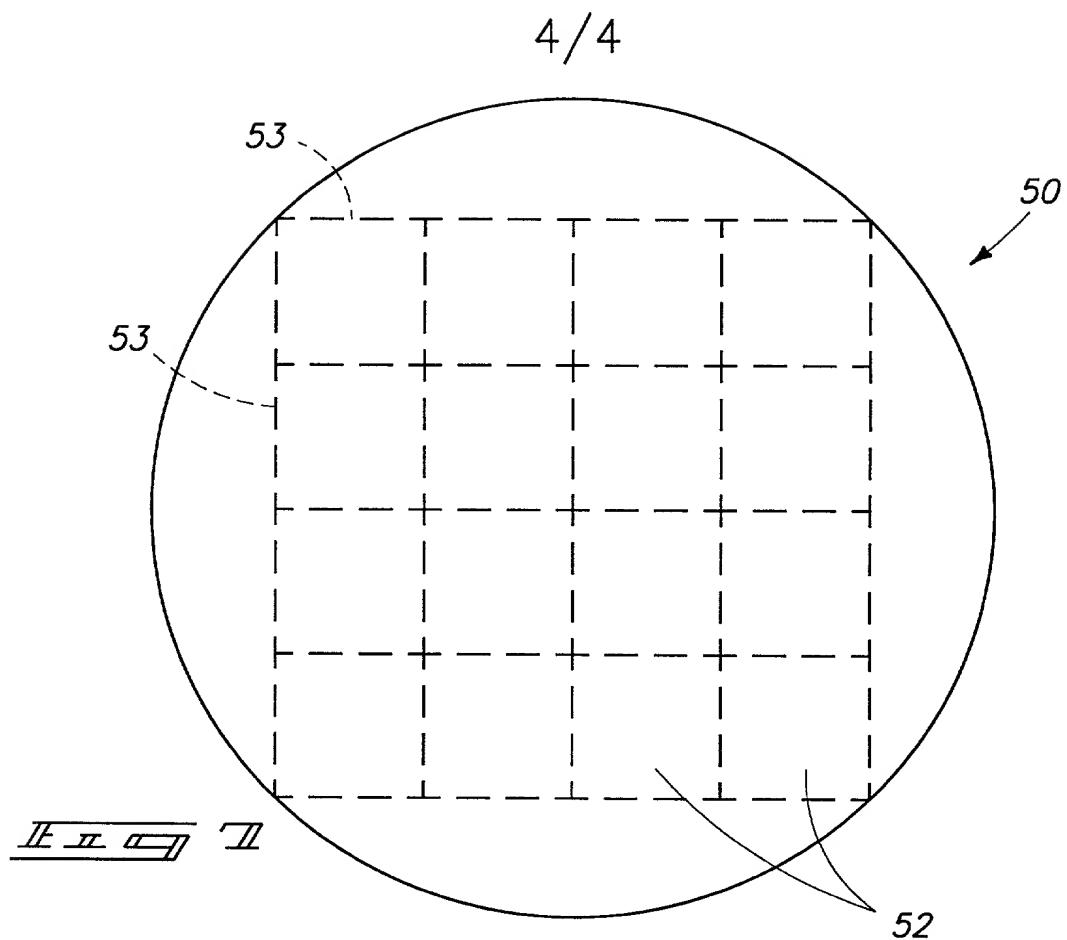
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DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

1 As the below named inventor, I hereby declare that:

2 My residence, post office address and citizenship are as stated below next
3 to my name.

4 I believe I am the original, first and joint inventor of the subject matter
5 which is claimed and for which a patent is sought on the invention entitled:
6 Semiconductor Processing Methods, the specification of which is attached hereto.

7 I hereby state that I have reviewed and understand the contents of the
8 above-identified specification, including the claims.

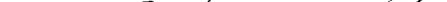
9 I acknowledge the duty to disclose information known to me to be material
10 to patentability as defined in Title 37, Code of Federal Regulations §1.56.

11 **PRIOR FOREIGN APPLICATIONS:**

12 I hereby state that no applications for foreign patents or inventor's
13 certificates have been filed prior to the date of execution of this declaration.

14 I hereby declare that all statements made herein of my own knowledge are
15 true and that all statements made on information and belief are believed to be
16 true; and further that these statements were made with the knowledge that willful
17 false statements and the like so made are punishable by fine or imprisonment, or
18 both, under Section 1001 of Title 18 of the United States Code and that such
19 willful false statement may jeopardize the validity of the application or any patent
20 issued therefrom.

Full name of inventor: Weimin Li

Inventor's Signature: 

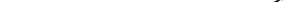
Date: Jan 14, 1888

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Full name of inventor: John Q. Li

Inventor's Signature: 

Date: 1-8-99

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